
AVR32102: Using the AVR32 SDRAM controller

Features

- Several types of SDRAMs supported
 - 2K, 4K or 8K row address memory parts
 - SDRAM with two or four internal banks
 - SDRAM 16 or 32 bit data path
 - CAS latency of 1,2 or 3 cycles supported
- Ease of use
 - Automatic refresh operation, programmable
 - Seamless access when configured
- Software configurable
 - Timing parameters
 - Initialization

1 Introduction

The AVR[®]32 has a dedicated SDRAM (Synchronous DRAM) controller. This controller is highly flexible and capable of supporting a series of external SDRAMs. Timing values and parameters are calculated from the SDRAMs datasheet and programmed into the SDRAM controller. This is also true for various types of access with respect to read and write operations. When the controller is correctly instantiated, the external SDRAM can then be accessed as a normal memory mapped device. The controller provides a seamless and transparent interface to a memory mapped SDRAM device.



32-bit **AVR[®]**
Microcontrollers

Application Note

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2 SDRAM Controller features

Several features are available in the SDRAM controller. These features can either be setup before normal operation begins, while other features can be enabled or disabled on the fly. The SDRAM controller is capable of either 16-bit or 32-bit data path, and supports byte, half-word and word access. Bursts can be used for both write and read access.

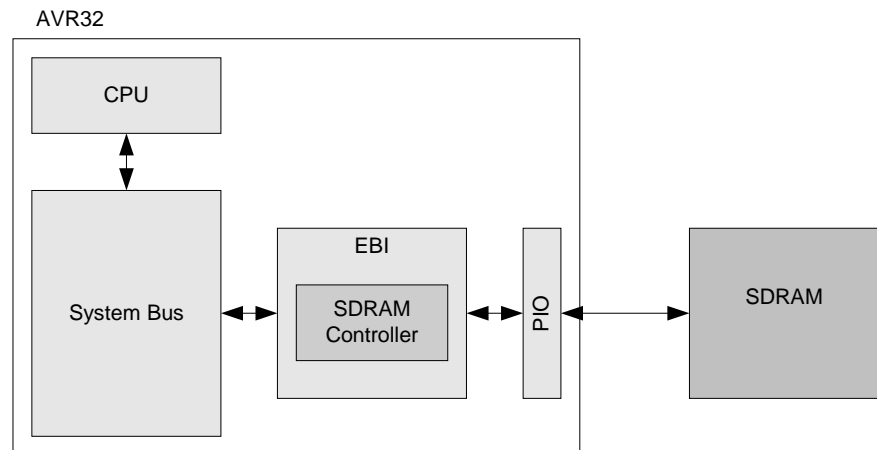
2.1 Device characteristics

A specific SDRAM device has device characteristics with respect to timing and command sequence. These device characteristics are stored into the SDRAM controller to control the data flow between the AVR32 and SDRAM. Once the SDRAM device is configured, the access to the SDRAM device is seamless to the user.

2.2 Access

The SDRAM Controller is part of EBI (External Bus Interface), which is accessed through the System Bus from the CPU core. In turn the SDRAM Controller may connect to an external SDRAM through the PIO. A conceptual schematic of the path is illustrated in Figure 1.

Figure 1: Conceptual schematics



In order to get access to the SDRAM all the parts along the path must be configured correctly to support the specific SDRAM.

3 Theory of operation and connectivity

Several terms and expressions are used when describing and working with SDRAM. This chapter will highlight the parts needed to configure your SDRAMC. This is by no means an extensive description on how SDRAMs work, but a brief introduction and description on the factors the SDRAM Controller has to take into account. For more information about SDRAM operation, consult the datasheet for AVR32 device or SDRAM datasheet.

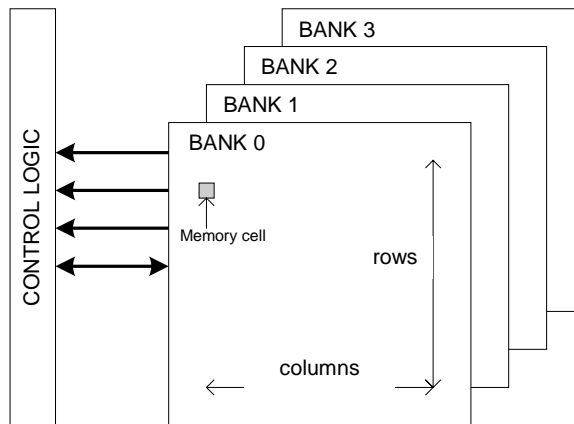
3.1 Response times

Whenever issuing a command (i.e. read/write, a bank/row/column change) a certain delay is associated with that command. These values are dependent on the SDRAM device chosen and can be found in the datasheet of the chosen device. The timing of control signals is also found in the datasheet.

3.2 Physical layout & Access

A SDRAM consists of DRAM memory blocks, which are called banks. Some devices have 2 banks, but the greater majority has 4. Each of these banks consists of a certain number of columns and rows to uniquely identify a memory cell. This is shown in Figure 3.1.

Figure 3.1: Generic SDRAM device



The number of columns and rows available multiplied by the number of banks (4) give the total memory size of the SDRAM. The address will consist of different parts for accessing a specific row and column within a bank. This configuration is similar for different sizes of SDRAM. An example is found in Table 1.

Table 1: SDRAM Configuration Mapping: 2048 rows, 4 banks

CPU Address Line																									
25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			BA[1:0]				Row[10:0]										Column[7:0]							NBS[1:0]	
			BA[1:0]				Row[10:0]										Column[8:0]							NBS[1:0]	
			BA[1:0]				Row[10:0]										Column[9:0]							NBS[1:0]	
BA[1:0]			Row[10:0]										Column[10:0]							NBS[1:0]					

Table 1 shows how the address lines (relative from the offset) are connected and how they are used in the SDRAM. The mapping shows how signals are used in a 8MB SDRAM.

A SDRAM may then be connected straightly to EBI interface as shown in Figure 3.2. Keep in mind that the Parallel I/O controller must be configured to gain access to the pins through the SDRAM Controller.



Figure 3.2: SDRAM connection

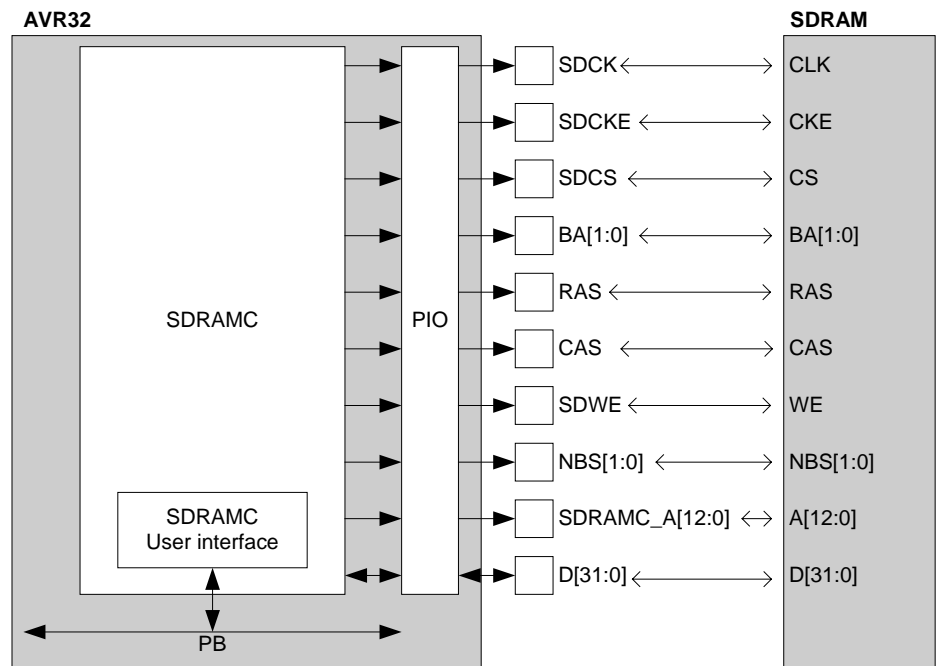


Figure 3.3: SDRAM connectivity

Instead of using a single SDRAM, multiple SDRAMs can be connected together to the SDRAMC to increase the amount of SDRAM available to the system. One possible solution is shown in Figure 3.4.

Figure 3.4: 2MB x 4 schematics

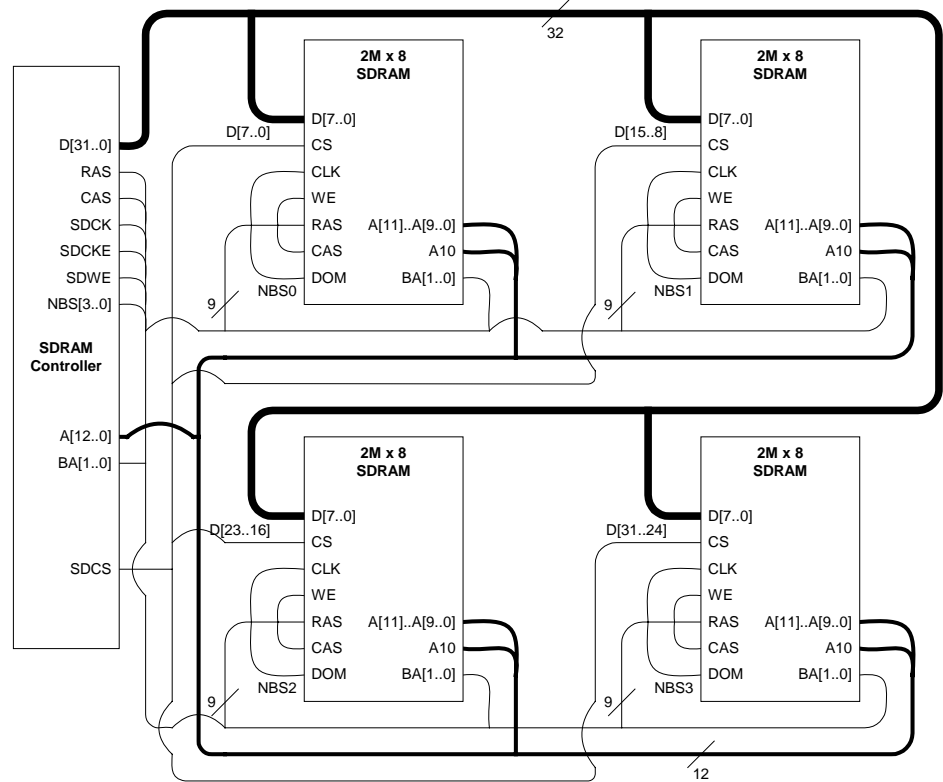


Figure 3.4 shows how 4 identical SDRAMs are connected in series. The 4 2MB SDRAMs provide a seamless 8MB memory segment. When creating such a series, it is of the utmost importance that the timing parameters are compatible for all the SDRAMs.

Most SDRAM has burst support as well. It is very common for a sequential read to be referred to as burst read with length one. Variants of bursts like sequential and interleaved bursts may also be available. These access types are usually written to the SDRAM Mode Register. Consult the SDRAM documentation for a list of features that your device supports. Chapter 4.3.1 describes how to issue these commands from the AVR32 to the SDRAM.

3.3 Data maintenance

As SDRAM consists of blocks of DRAM, the data must be refreshed at intervals to maintain the data integrity. This interval is specified in the datasheet for the selected SDRAM device. If the data is not refreshed at a regular interval, the data may become of an unknown state.



4 SDRAM controller

The SDRAM controller must be configured to match the timing characteristics of the specified device before usage. This chapter covers this configuration.

4.1 Initialization

After a reset, the AVR32 is not configured to access an external SDRAM device. The sequence for initializing the SDRAM controller after a successful reset will be as follows:

- Setup the HMATRIX to enable SDRAMC.
- Initialize the SDRAMC and timing characteristics for your specific device
- Configure your parallel input/output Controller (PIO Controller)

4.2 HMATRIX

The SDRAM is connected to the EBI. The HMATRIX is the AHB Bus Matrix that connects every controller on the bus to the AVR32 CPU. The SDRAMC is not selected by default, but it will have to be enabled. This is done by setting one of the special function registers for your device. The registers are named sfrX and are found in the HMATRIX module.

4.3 SDRAM registers and user interface

To specify the access type and timings for the SDRAM, the SDRAMC registers are used. The registers listed here must be configured to make sure your SDRAM will work correctly. There are other registers as well; for more information about these register and more in depth description concerning the registers described in this section, consult your AVR32 datasheet.

4.3.1 SDRAMC_MR: Mode Register

The value SDRAMC_MR defines the command issued when the SDRAM is accessed. This is written directly to the mode register. This is a 3 bit value with the following commands available:

Table 2: SDRAM commands

Mode			Description
0	0	0	Normal access
0	1	1	Issues a NOP-command regardless of cycle
0	1	0	All Banks Precharge regardless of cycle
0	0	1	Load Mode Register. Whenever this mode is selected, the access to "SDRAM-Base +offset" address will write the value "offset" to the SDRAM device Mode register.
1	0	0	An Auto-Refresh command. An "All Banks Precharge" must be issued previous to this command.
1	0	1	Extended Load Mode Register. This is equivalent to "Load Mode Register".
1	1	0	Deep power-down mode

4.3.2 SDRAMC_TR: Refresh Timer Register

The Refresh Timer Register (SDRAMC_TR) contains the number of clock cycles (period) of the refresh pulse. This value is dependent on Master Clock Frequency, the refresh rate of the SDRAM device and the refresh burst length. 15,6 μ s per row is a typical value for a burst length of one. This is 12-bit value that reflects which has denomination in clock cycles.

4.3.3 SDRAMC_CR: Control Register

The Configuration Register (SDRAM_CR) contains information about timing and physical characteristics of the selected SDRAM-device:

Table 2: SDRAMC Control Register

Bit / bitfield	Description
NC	Number of columns
NR	Number of rows
NB	Number of banks
CAS	CAS latency
DBW	Data bus width
TWR	Write recovery delay. The write recovery delay in clock cycles
TRC	Row cycle delay. The delay between a Refresh and an Activate Command in cycles.
TRCD	Row to column delay. The number of cycles between a Precharge Command and a tailing Command.
TRAS	Active to Precharge delay. This field contains the delay (in clock cycles) between an Activate Command and a Read/Write Command.
TXSR	Exit Self Refresh to Active Delay. The number of clock cycles between SCKE high and Activate Command is defined as TXSR.

Please note that all these fields have a default reset value that may or may not correspond to your SDRAM. These values can either be found, or calculated from, the SDRAM manufacturer's datasheet.

4.3.4 SDRAMC_HSR: High Speed Register

The High Speed Register contains a single bit, DA, which enables or disables decoding of cycles.



4.3.5 SDRAMC_LPR: Low Power Register

The Low Power Register enables low power features to be applied to the SDRAM device.

Table 3: Low Power Register

Bitfield	Size	Description	Only low-power SDRAM
LPCB	2	Low Power configuration bits	
PASR	3	Partial Array Self-refresh. Used during initialization to specify whether only one quarter, one half quarter or all banks is to be enabled. Disabled banks are not refreshed	*
TCSR	2	Temperature Compensated Self-refresh. Used during initialization to set the refresh timer interval according to temperature. Consult your SDRAM datasheet for more information	*
DS	2	Drive Strength. Check your SDRAM device specification.	*
TIMEOUT	2	Define when low-power mode is enabled	

The LPCB may be configured in one out of 4 ways:

- 00: Low Power Features inhibited.
- 01: Issues a Self Refresh Command to the SDRAM device. SDCLK is deactivated and SDCKE is set low. The SDRAM device is always in Self-refresh mode while not accessed.
- 10: Issues a Power-down Command to the SDRAM device. SDCKE is set low. The SDRAM device is always in Power-down mode while not accessed.
- 11: Issues a Deep Power-down mode to the SDRAM device. Unique to low-power SDRAMs.

The TIMEOUT bitfield defines when low-power mode is enabled and may have one of the following values:

- 00: Activate low-power mode immediately after the end of the last transfer.
- 01: Activate low-power mode 64 clock cycles after the last transfer.
- 10: Activate low-power mode 128 clock cycles after the last transfer.
- 11: Reserved.

4.3.6 Interrupt registers

All interrupt registers have one bit that enables the actual feature (high) or disables it (low).

Table 4: SDRAMC interrupt registers

Register	Description
SDRAMC_IER	Interrupt Enable Register. Enables refresh error interrupt.
SDRAMC_IDR	Interrupt Disable Register. Disables the refresh error interrupt.
SDRAMC_IMR	Interrupt Mask Register. Mask the refresh error interrupt or not.
SDRAMC_ISR	Interrupt Status Register. Is read as true if a refresh error interrupt has occurred since this register was last read.

4.3.7 SDRAMC_MDR: Memory Device Register

In the Memory Device Register it is specified the type of SDRAM used. It has a single bitfield, MD, which specifies the type and is 2 bits long. The bitfield Memory Device Type (MD) can have one of the following values:

- 00: SDRAM
- 01: Low-power SDRAM
- 10: Reserved
- 11: Reserved

4.4 EBI and PIO

The SDRAMC is part of the EBI interface. To get the EBI interface out on the I/O-pins, the correct module must be set for the PIO controller. This is done by activating the appropriate module for the PIO port.

4.5 Usage

When the SDRAM controller is correctly initialized, the physical lines are connected and the correct module has control over the PIO lines, the SDRAM is ready to go. The EBI interface have it's own dedicated memory space. All devices connected to the AVR32 through the EBI can thus be memory-mapped. The appropriate base address for the EBI can be found in the datasheet. All access to the memory area that covers the SDRAM is then transparent.



5 Package information

Included with the application note is a driver package. This package contains drivers, example code and documentation.

5.1 Drivers

Drivers are available in the package. These drivers are written to be independent of a specific compiler and are successfully tested on GCC (GNU Compiler Collection) and IAR Embedded Workbench®. This example is for the SDRAM found on the STK1000.

5.2 Examples

Examples are available from the corresponding driver package. All functionality is divided into libraries and an example that utilizes the library.

5.3 Documentation

Function specific documentation is available in the package. Refer to [readme.html](#).



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